Exhibit C

Docket No.: 635162800300
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Inter Partes Reexamination of:
Jayesh BHAKTA et al.

Control Nos.: 95/001,339; 95/000,578; 95/000,579

Filed: October 20, 2010; October 21, 2010; June 8, 2010

For: MEMORY MODULE DECODER

Examiner: B. PEIKARI

Art Unit: 3992

Conf. No.: 5035; 8810; 3547

SECOND SUPPLEMENTAL DECLARATION OF DR. CARL SECHEN UNDER 37 C.F.R. § 1.132

Mail Stop Inter Partes Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Dr. Carl Sechen, declare as follows:

1. I have been retained by Netlist, Inc., the owner of U.S. Patent No. 7,619,912 ("the '912 patent") to provide a supplemental technical opinion concerning the '912 patent, and certain prior art references cited in the above-captioned *inter partes* reexamination proceedings, which are discussed in further detail below.

2. In my initial declaration dated July 5, 2011, I summarized my technical background and provided my then current Curriculum Vitae. For this supplemental declaration, I am providing an updated Curriculum Vitae as Exhibit AAA.

3. I have reviewed and am familiar with the specification of the '912 patent. I have also reviewed and am familiar with the Decision On Appeal issued by the Patent and Trial Appeal Board (the "Board") and mailed on May 31, 2016 ("the Decision").

8. Moreover, I explain that the prior art applied by the Decision in its new grounds of rejections at least fail to disclose or suggest the claimed inventions as amended in Patent Owner's Decision Response.

9. I address each of these issues separately below.

I. Claim Amendments

A. Phase Lock Loop (PLL) Device

10. I understand that claim 1 is amended to include claim language for a PLL clock signal. The claim language, including citations to the '912 Patent in which a POSITA can find exemplary support, is presented below (addition amendments underlined and support citations in curly braces):

> a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> wherein, in response to signals received from the computer system {5:28}, the phase-lock loop (PLL) device {50 in Figs. 1A, 1B} transmits a PLL clock signal {5:29} to the plurality of DDR memory devices, the logic element, and the register {5:29-31}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations.

B. Register

11. I understand that claim 1 is amended to include claim language for the register. The claim language, including citations to the '912 Patent in which a POSITA can find exemplary support, is presented below (addition amendments underlined and support citations in curly braces):

> a register…
>
> wherein, the register {60 in Figs. 1A, 1B} (i) receives, from the computer system {5:31}, and (ii) buffers, in response to the PLL clock signal {Figs. 1A, 1B; 5:31}, a plurality of row/column address signals {7:43-45} and the bank address signals {7:50-51}, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices {30 in Figs. 1A, 1B; 5:34-36}, wherein the at least one row/column address

> signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register {A_0-A_n in Figs. 1A, 1B} are separate from the at least one row address signal received by the logic element {A_{n+1} in Figs. 1A, 1B}[.]

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations.

C. Logic Element

12. I understand that claim 1 is amended to include claim language for the logic element. The claim language, including citations to the '912 Patent in which a POSITA can find exemplary support, is presented below (deletion amendments bracketed, addition amendments underlined, and support citations in curly braces):

> the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, …
>
> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals {Figs. 1A, 1B, 3A, 3B; 17:28-19:52l 22:50-63; 23:6-25} of the output control signals in response {6:55-63} at least in part to (i) the at least one row address signal {A_{n+1} in Figs. 1A, 1B; A13 in Figs. 3A, 3B; 7:46-53}, (ii) [a] the bank address signals {B_0-B_m in Figs. 1A, 1B; BA_0, BA_1 in Figs. 3A, 3B; 7:46-53}, and (iii) the at least one chip-select signal {CS_0, CS_1 in Fig. 1A; CS_0 in Fig. 1B; 7:46-53} of the set of input control signals and (iv) the PLL clock signal {Figs. 1A, 1B; 5:29-30; "clk_in" in 17:28-19:52}.

Claims 15, 28, 39, 52, 67, 77, 82 and 87 have identical or nearly identical recitations.

D. Other Amendments

13. I understand that Patent Owner has made other claim amendments conform the claim language to the above main claim amendments.

II. Amidi In View Of Dell 2 – Claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122 and 132-136 (Ground 5)

14. I have been informed that claims 1, 3, 4, 6, 8, 10-15, 18-20, 22, 24, 25, 27-29, 31, 32, 34-43, 45-50, 120-122 and 132-136 have been rejected by the Decision as obvious over

Amidi in view of Dell 2. I confirm that the amended claim language introduced by the Decision Response distinguishes these claims for this combination of Amidi and Dell 2, as will be discussed below.

15. I have been informed that the Decision concludes that the combination of Amidi and Dell 2 teaches or suggests generating a chip-select, CAS, or rank selecting signal in response to a bank address signal. The Decision refers to its discussion at pages 40-43 of the bank address limitation with respect to claim 7 to support this conclusion. (Decision, 81.) I have also been informed the Decision bases the rejection on the breadth of the claims. In particular, the Decision states:

> The above teachings in Dell 2 teach or suggest a logic element receiving and using free signals, including a bank address signal, to provide the needed bank address signals based on the difference between the actual and expected number of banks for the memory devices of the memory module system. Combining this teaching with Amidi' s suggestion to use other types of memory devices (Amidi ¶ 71) would have predictably yielded the recited "both the bank address signals of the set of input control signals are received by both the logic element and the register" in claim 7 so that the necessary rank chip select signals discussed in Amidi are produced. That is, Amidi and Dell 2, collectively, teach that ranks and banks both may be expanded; therefore, a skilled artisan would recognize various combinations of inputs to achieve expansion including bank address inputs as broadly recited. This combination also addresses the demand for increased memory capacity and compatibility issues. *See, e.g.*, R2 August 14, 2013 Comments 12 (citing 3d Bagherzadeh Decl. ¶ 37), 29-30, 38 (citing Amidi ¶ 71). Moreover, this combination further teaches using the logic circuit or element (e.g., Amidi's CPLD) to receive bank address signals for the above-discussed purpose.
>
> (Decision, 43.)

16. As discussed above, the claims have been amended to include language about the PLL, register, and logic element. A POSITA would understand that the amendments narrow the scope of the claim to a memory module in which the bank address signals are received by the register (and thereby the plurality of DDR memory devices) and the logic element, and at least

one row address signal – *separate* from the plurality of row/column address signals received by the register – is received by the logic element. A POSITA would understand that for such a configuration, generating a CAS signal or a chip-select signal in response at least in part to the bank address signals and the at least one row address signal is nonobvious in view of Amidi and Dell 2, as discussed in more detail below.

17. In particular, I see that the amended claims now require in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register. I also see the amended claims now require that the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal. Additionally, I see that the amended claims now require that the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element.

18. Such language, individually and in combination, distinguishes these claims from the combination of Amidi and Dell 2. First, Amidi's CPLD does not generate output control signals in response to the PLL clock signal. As amended, the claims require the PLL device transmit a PLL clock signal to the logic element, in response to signal received from the computer system, and the logic element generates gated CAS signals or chip-select signals in response at least in part to the PLL clock signal. By providing a PLL clock signal from the PLL 50 to the plurality of DDR memory devices, the logic element 40 and the register 60, the memory module of claim 1 of the '912 patent is configured to provide reliable synchronous operation. (*See* Sechen I, ¶ 16.) Such language distinguishes these claims from Amidi, which transmits the PLL clock signal to the register and memory, but not to the CPLD.

23. Even taking Amidi in combination with Dell 2, it would not be obvious to a POSITA to modify Amidi's system to provide bank address signals to the CPLD device, and generate control signals based thereon. The rejection of the claims relies on Amidi's use of Add(n) to generate the control signals. Amidi, for example, provides an address signal, Add(n), to the CPLD 604 that decodes Add(n) with inputs CS0 and CS1 to generated output signals rCS0-rCS3. (Amidi Fig. 5.) Add(n) is not transmitted to the memory devices (and can be used by Amidi for rank multiplication). There is no suggestion in Amidi to use a bank address signal for generation of control signals. Amidi does not discuss any rationale for making this modification, because Amidi's CPLD is alleged to be fully functional without receiving any bank address signals. For example, Amidi discloses the internal circuitry of the CPLD – which does not utilize any bank address signals. (Amidi, ¶ 64-70, Fig. 8.) Instead, Amidi discloses that the register receives the bank address signals so that they can be passed through to the DDR memory devices for their normal function of specifying the bank from which data is to be read or written. Furthermore, there is no suggestion or recognition in Amidi or Dell 2 to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals.

24. As amended, the claims are narrowed in scope such that a POSITA would understand that at least one row address signal is received by the logic element and not received by the register, but that the bank address signals are received and used by the plurality of memory devices (e.g., during an activate command, a read command or a write command). In particular, the claims require that the *logic element receives* at least one row address signal and *bank address signals*, and require that *the register* (i) *receives*, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and *the bank address signals*, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices. The claims also require the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element. In other words, in the configuration recited by the claims, the bank address signals are received by the logic element, the register and the plurality of memory devices. Under such circumstances, Amidi does not use bank address signals to generate control signals (and certainly not the bank address signals and

the at least one row address signal). The claims, however, require generating CAS signals or chip-select signals based on a row address signal and bank address signals.

25. Dell 2 discloses a remapping or reassignment of a row address bit (A12) to be used as a bank address bit (BA1). There is no disclosure or suggestion of using bank address to generate a control signal, such as a chip-select signal or a CAS signal. (Sechen I, ¶¶ 27, 73; Sechen II, ¶ 16.)

26. Taking Amidi and Dell 2 together for all that they teach, it would not be obvious to a POSITA to use bank address signals to generate control signals for rank multiplication, when the bank address signals are used by the plurality of memory devices. As amended, the narrower claim dictates that a row address signal, and not a bank address signal, is received by the logic element separate from the signals received by the registers. Amidi and Dell 2 at best would suggest to a POSITA to use such a signal (i.e., one that is received separate by the logic element and not by the registers) for generating a control signal. There is no suggestion to repurpose a bank address signal for rank multiplication purposes. Certainly, there is no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal signals.

27. Based on the above, I find that it would not be obvious to a POSITA to combine Amidi and Dell 2 to reach the claimed invention, as amended. For the sake of argument, however, even the proposed combination of Amidi and Dell 2 fails to disclose the claimed invention. Therefore, even in combination, Amidi in view of Dell 2 fails to disclose all of the claim recitations of the claims.

III. Micron In View Of Amidi – Claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 (Ground 13)

28. I have been informed that claims 1, 3, 4, 6, 8, 10, 11, 15, 18-20, 22, 24, 25, 27-29, 31, 32, 36-39, 41-43, 45, 50, 52-54, 56, 58, 60-63, 67-71, 75, 77-93, 109-111, and 120-136 have been rejected by the Decision as obvious over Micron in view of Amidi. I confirm that the

statements made on information and belief are believed to be true; and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: July 31, 2016

Carl Sechen, Ph.D.